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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/538,212	06/09/2005	Erwin A Hijzen	NL 021417	1812

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
ULLAH, ELIAS	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/538,212	HIJZEN ET AL.	
	Examiner	Art Unit	
	Elias Ullah	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/538,212.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/7/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to amended application filled on 11/17/2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Murphy US 6,444,528 dated 11/3/2002.

4. With respect to claim 1, Murphy shows the method as claimed in figures Fig. 1-7 and corresponding text, as: a method of manufacturing a trench gate semiconductor device comprising the steps of: providing a silicon device body (Fig.2, refer to complete drawing is a device body) having a first major surface (above the trench 10 area), the silicon device body (16) having a drain region (16) of a first conductivity type and a body region (22) over the drain region; forming a trench (10) extending downward into the silicon device body (Fig. 2) from the first major surface, the trench having sidewalls (Fig.3, 35) and base (36); depositing a nitride liner (40) with in the trench to protect the sidewalls; forming a polysilicon plug (15, col. 1, lenses 26-30) at the base of the trench; thermally oxidizing the device (col. 3, lines 38-40) to oxidize the polysilicon at the

bottom of the trench to from an oxide plug (col. 2, lines 45-50); and depositing conductive material within the trench to from a gate (col.3, lines 38-42).

5. With respect to claim 2, Murphy also shows the method as claimed in corresponding text, as: the step of forming a polysilicon plug at the base of the trench (col. 3, lines 40-45).

6. With respect to claim 3, Murphy shows the method as claimed in figures Fig. 1-7 and corresponding text, as: depositing a doped polysilicon plug (15) at the base of the trench includes depositing polysilicon over the first major surface including at the trench (10, Fig. 2) and then etching back the doped polysilicon to remove the doped polysilicon form the first major surface leaving the polysilicon at the abase of the trench (Fig. 3, Poly-silicon is inherent in this process, because it form gate electrode for the device)

7. With respect to claim 5, Murphy also shows the method as claimed in figures Fig. 1-7 and corresponding text, as: Thermally oxidizing the side wall of the trench to form an oxide layer before depositing the nitride liner over the oxide layer (42); etching away the nitride liner and the oxide layer (col. 4, lines 43-45) after the doped oxidizing the doped polysilicon (oxidizing is taken place before etch steps see col. 2, lines 48-50 and lines 56-58) ; and thermally oxidizing the sidewalls to form a thermal oxide gate insulator before depositing conductive material within the trench to from a gate (col. 1, lines 25-30. 15)

8. With respect to claim 6, Murphy also shows the method as claimed in corresponding text, as: the stop of forming the trench includes providing a mask on the

first major surface defining an opening and etching through the opening a trench extending downwards from the first major surface (col. 4, lines 24-30)

9. With respect to claim 7, Murphy also shows the method as claimed in corresponding text, as: the mask is an oxide hard mask (col. 4, lines 24-30).

10. With respect to claim 8, Murphy also shows the method as claimed in corresponding text, as: the steps of depositing conductive material to form a gate includes filling the trench with polysilicon to form a gate (col.1, lines 28-30).

11. With respect to claim 9, Murphy also shows the method as claimed in corresponding text, as: Forming a source implant of first conductivity type at the first major surface adjacent to the trench and forming source (col. 1, lines 35-38), gate and drain electrodes attached to the source implant, the gate and the drain region respectively to complete the trench gate semiconductor device (Fig. 1, col. 1, lines 30-40).

12. With respect to claim 10, Murphy shows the method as claimed in figures Fig. 1-7 and corresponding text, as: a trench MOSFET comprising: a drain region (16) of first conductivity type; a body region over the drain region (22); a trench extending from a first major surface through the body region (col. 1, lines 30-32); source region (14) laterally adjacent to the trench at the first major surface; thermal gate oxide (12) on the side walls of the trench; a gate electrode in the trench insulated from the body region by the gate oxide (12); characterized by a thick oxide plug (42) formed of oxidized doped polysilicon at the base of the trench extending into the drain region (col. 2, lines 45-50).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murphy (6,444,528) in view of Tsang et al. (US 6,326,261 dated 12/04/2001).

14. With respect to claims 4, Murphy shows the method as claimed and as described in preceding paragraphs, but Murphy does not expressly disclose depositing doped polysilicon includes depositing un-doped polysilicon and then carrying out a diffusion process to doped the un-doped polysilicon.

15. Tsang et al. discloses introducing doped polysilicon includes depositing un-doped polysilicon and then carrying out a diffusion process to dope the un-doped polysilicon (col. 4, lines 48-54) to from a gate. In view of this disclosure, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make conductive gate with polysilicon layer of Murphy because such a process is use to form a gate of a transistor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elias Ullah whose telephone number is 571-272-1415. The examiner can normally be reached on 8-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MICHAEL LEBENTRITT can be reached on (571)272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER

EMU